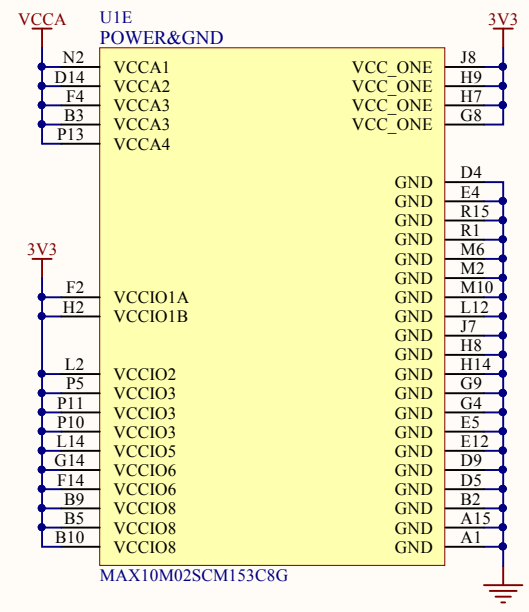
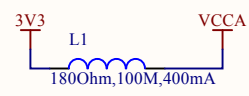
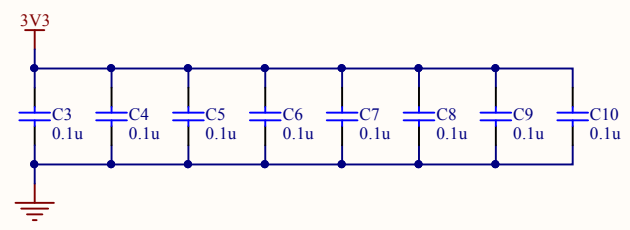
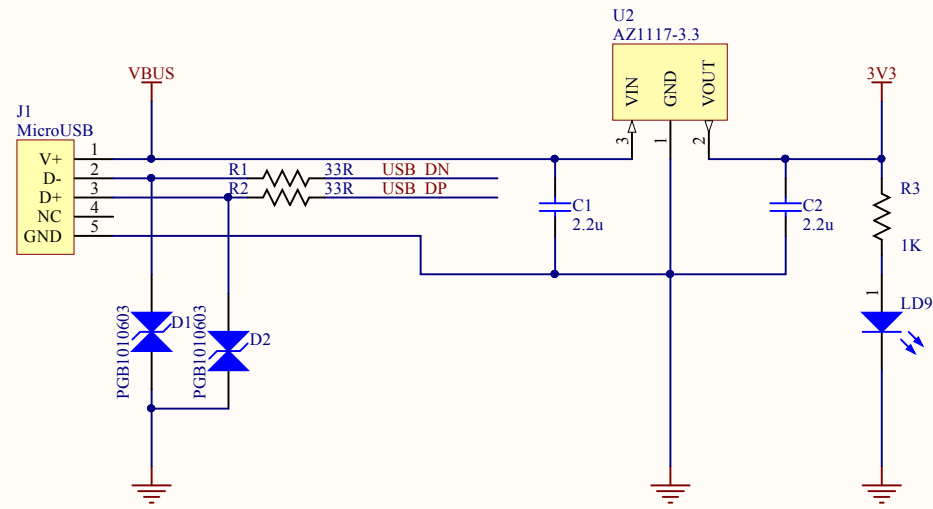


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BANK 1A&1B&2

DIFFIO\_RX\_L1n D2 SEG-B1  
 DIFFIO\_RX\_L1p C2 SEG-G2  
 DIFFIO\_RX\_L3n F5 SEG-F1  
 DIFFIO\_RX\_L3p G5 SEG-G1  
 DIFFIO\_RX\_L5n C1 SEG-F2  
 DIFFIO\_RX\_L5p B1 SEG-DIG2  
 DIFFIO\_RX\_L7n E1 SEG-A1  
 DIFFIO\_RX\_L7p E2 SEG-DIG1

JTAGEN G7 JTAGEN  
 DIFFIO\_RX\_L11n/TMS G1 TMS  
 VREFB1N0 G2 SEG-E1  
 DIFFIO\_RX\_L11p/TCK J1 TCK  
 DIFFIO\_RX\_L12n/TDI H5 TDI  
 DIFFIO\_RX\_L12p/TDO H4 TDO  
 DIFFIO\_RX\_L14n H3  
 DIFFIO\_RX\_L14p J2 SEG-D1  
 DIFFIO\_RX\_L16n L1 SEG-DP1  
 DIFFIO\_RX\_L16p K2 SEG-C1

BANK 2

DIFFIO\_RX\_L18n/CLK0n J4  
 DIFFIO\_RX\_L18p/CLK0p J5  
 DIFFIO\_RX\_L20n/CLK1n K5  
 DIFFIO\_RX\_L20p/CLK1p K4  
 DIFFIO\_RX\_L22n/DPCLK0 L5  
 VREFB2N0 P1 SEG-D2  
 DIFFIO\_RX\_L22p/DPCLK1 L4  
 R2 SEG-DP2  
 DIFFIO\_RX\_L27n/PLL\_L\_CLKOUTn N1 SEG-E2  
 DIFFIO\_RX\_L27p/PLL\_L\_CLKOUTp P2 SEG-C2

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BANK 5&6

DIFFIO\_RX\_R2p N15 LED1  
 DIFFIO\_RX\_R2n N14 LED2  
 M14 LED3  
 DIFFIO\_RX\_R1p M12 LED4  
 VREFB5N0 L15 LED5  
 DIFFIO\_RX\_R7n K12 LED6  
 DIFFIO\_RX\_R1n L11 LED7  
 DIFFIO\_RX\_R7p K11 LED8  
 DIFFIO\_RX\_R10p J9 KEY1  
 DIFFIO\_RX\_R11p K14 KEY2  
 DIFFIO\_RX\_R10n J11 KEY3  
 DIFFIO\_RX\_R11n J14 KEY4

DIFFIO\_RX\_R14p/CLK2p J12 SW1  
 DIFFIO\_RX\_R14n/CLK2n H11 SW2  
 DIFFIO\_RX\_R16p/CLK3p H12 SW3  
 DIFFIO\_RX\_R16n/CLK3n H13 SW4  
 DIFFIO\_RX\_R18p J15  
 DIFFIO\_RX\_R18n G15 R-LED1  
 DIFFIO\_RX\_R26p/DPCLK3 G11  
 VREFB6N0 E15 G-LED1  
 DIFFIO\_RX\_R26n/DPCLK2 G12  
 E14 B-LED1

DIFFIO\_RX\_R27p F11  
 DIFFIO\_RX\_R28p C15 R-LED2  
 DIFFIO\_RX\_R27n F12  
 DIFFIO\_RX\_R28n C14 G-LED2  
 DIFFIO\_RX\_R33p E11  
 DIFFIO\_RX\_R33n D12 B-LED2

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BANK 3

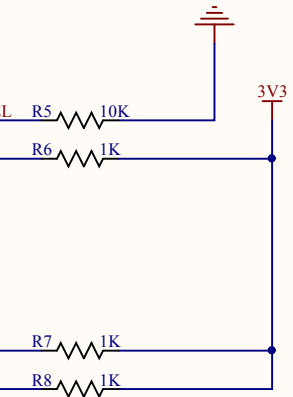
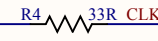
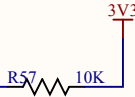
DIFFIO\_TX\_RX\_B1n M4 GPIO0  
 DIFFIO\_RX\_B2n P3 GPIO1  
 DIFFIO\_TX\_RX\_B1p M5 GPIO2  
 DIFFIO\_RX\_B2p R3 GPIO3  
 DIFFIO\_TX\_RX\_B3n L6 GPIO4  
 DIFFIO\_RX\_B4n P4 GPIO5  
 DIFFIO\_TX\_RX\_B3p L7 GPIO6  
 DIFFIO\_RX\_B4p R5 GPIO7  
 DIFFIO\_TX\_RX\_B5n P6 GPIO8  
 DIFFIO\_RX\_B6n R7 GPIO9  
 DIFFIO\_TX\_RX\_B5p P7 GPIO10  
 DIFFIO\_RX\_B6p P8 GPIO11  
 DIFFIO\_TX\_RX\_B7n L8  
 DIFFIO\_RX\_B8n P9 GPIO12  
 DIFFIO\_TX\_RX\_B7p M7  
 DIFFIO\_RX\_B8p R9 GPIO13  
 DIFFIO\_TX\_RX\_B9n M8  
 VREFB3N0 R11 GPIO14  
 N8  
 DIFFIO\_TX\_RX\_B9p P12 GPIO15  
 R14 GPIO16  
 P15 GPIO17

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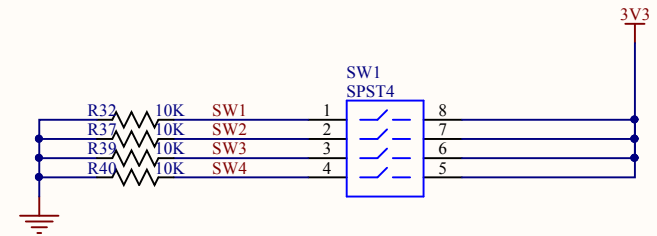
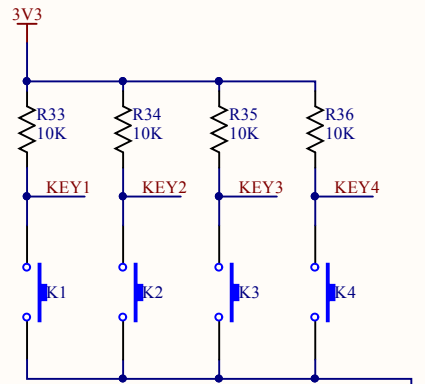
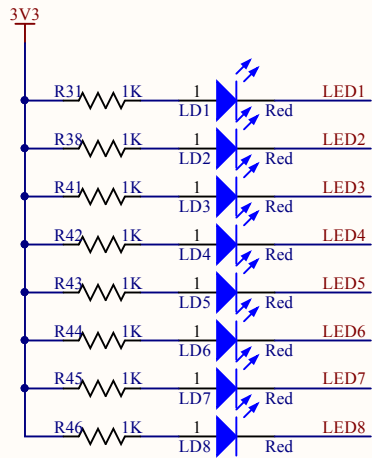
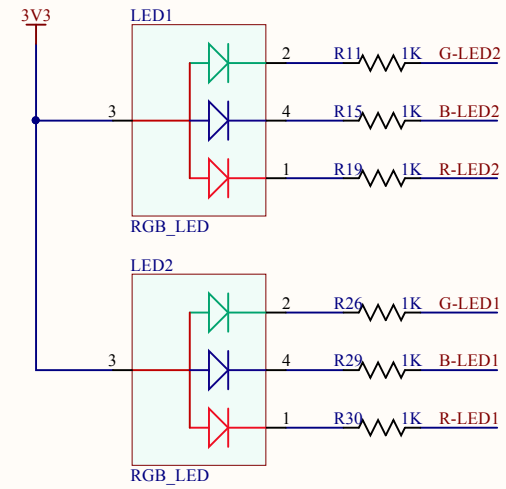
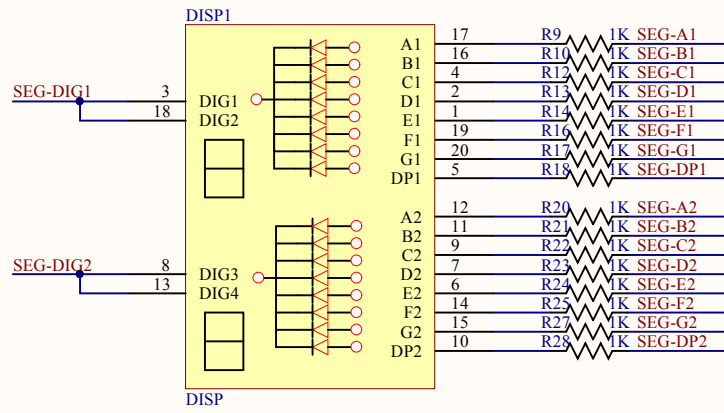
BANK 8

DIFFIO\_RX\_T14p D11  
 DIFFIO\_RX\_T15p B15 GPIO18  
 DIFFIO\_RX\_T14n D10 GPIO26  
 DIFFIO\_RX\_T15n B14 GPIO19  
 DIFFIO\_RX\_T16p C8 GPIO28  
 DIFFIO\_RX\_T16p B13 GPIO20  
 DIFFIO\_RX\_T17p B8 GPIO27  
 DIFFIO\_RX\_T16n/DEV\_CLRn A14 GPIO21  
 DIFFIO\_RX\_T17n E10  
 DIFFIO\_RX\_T18p/DEV\_OE E9  
 DIFFIO\_RX\_T18n VREFB8N0 A13 GPIO23  
 CONFIG\_SEL D8 CONFIG SEL  
 DIFFIO\_RX\_T19p B12  
 nCONFIG E8  
 DIFFIO\_RX\_T19n B11 GPIO22  
 DIFFIO\_RX\_T20p B7 GPIO29  
 DIFFIO\_RX\_T21p A9 GPIO25  
 DIFFIO\_RX\_T20n B6 GPIO32  
 DIFFIO\_RX\_T21n A11 GPIO24  
 DIFFIO\_RX\_T22p D7 GPIO30  
 DIFFIO\_RX\_T23p A7 GPIO33  
 DIFFIO\_RX\_T22n/CRC\_ERROR E7 GPIO31  
 DIFFIO\_RX\_T23n A5 GPIO34  
 DIFFIO\_RX\_T24p/nSTATUS D6  
 B4 GPIO35  
 E6  
 DIFFIO\_RX\_T24n/CONF\_DONE A2 SEG-B2  
 DIFFIO\_RX\_T26p A3 SEG-A2  
 DIFFIO\_RX\_T26n

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